奇美電子 CHIMEI INNOLUX

PRODUCT SPECIFICATION

☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: V320HH6
SUFFIX: PSA

Customer:

APPROVED BY **SIGNATURE**

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Vincent Chou	Kevin Tsai

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 1.0	Jan. 21, 2010	All	All	The preliminary specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V320HH6-PSA is a 32.0" TFT Liquid Crystal Display module with Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit).

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	32.0
Pixels [lines]	1920 × 1080
Active Area [mm]	698.4(H) x 392.85(V) (32.0")
Sub-Pixel Pitch [mm]	0.12125 (H) x 0.36375 (V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 2100g
Physical Size [mm]	716.1(W) × 410(H) × 1.79(D) Typ.
Display Mode	Transmissive mode / Normally White
Contrast Ratio	1000:1 Typ. (Typical value measure at CMO's module)
Viewing Angle (CR>10)	160°(H)/150°(V) (CR>10) TN Technology (Typical value measure at CMO's module)
Color Chromaticity	R = (0.647, 0.328) G = (0.279, 0.633) B = (0.154, 0.058) W= (0.280, 0.290)
Cell Transparency [%]	5.10%
Polarizer Surface Treatment	Anti-Glare coating (Haze 25%)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight		2100		g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

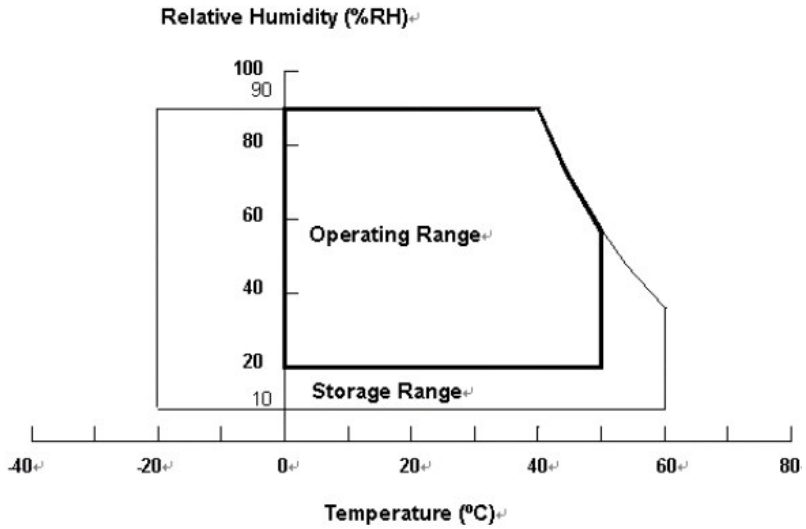
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stroed in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	VW	—	3000	VRMS	
Power Supply Voltage	VBL	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and Internal PWM Control.

3. ELECTRICAL CHARACTERISTICS

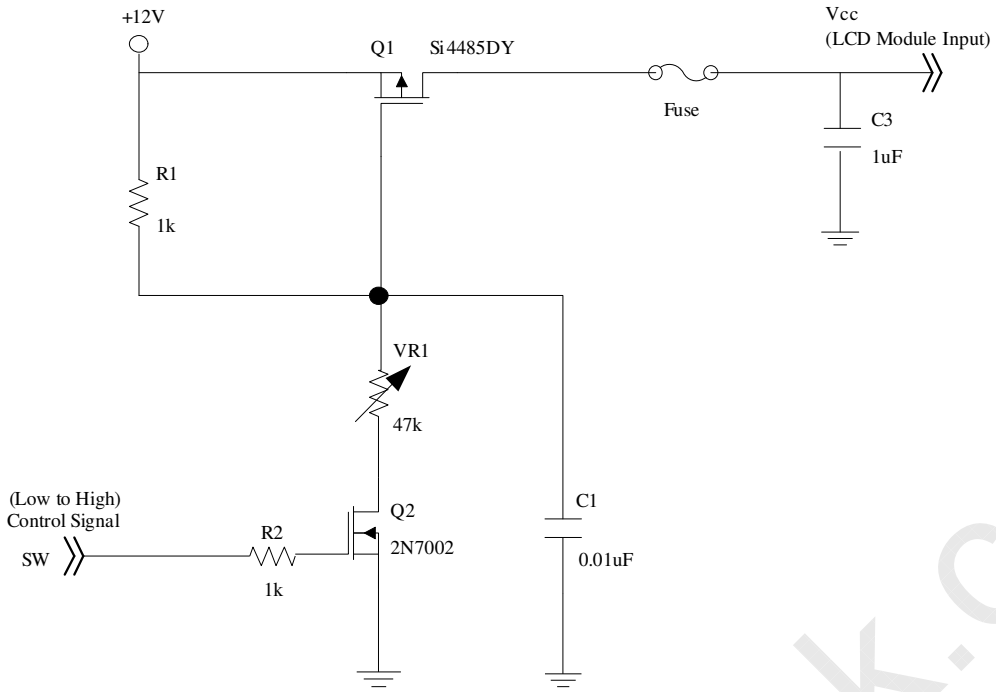
3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

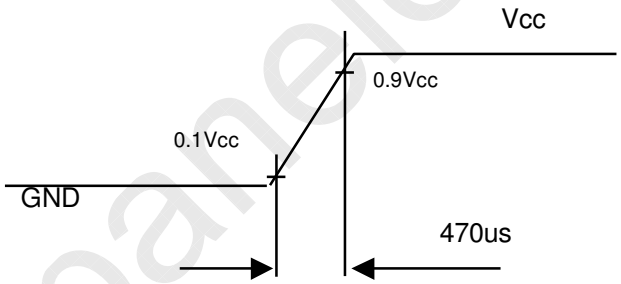
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	(13.2)	V	(1)
Rush Current		I_{RUSH}	—	—	(4)	A	(2)
Power Consumption	White Pattern	—	—	(6.6)	(7.8)	W	(3)
	Horizontal Stripe	—	—	(15)	(17.4)	W	
	Black Pattern	—	—	(15)	(17.4)	W	
Power Supply Current	White Pattern	—	—	(0.55)	(0.65)	A	
	Horizontal Stripe	—	—	(1.25)	(1.45)	A	
	Black Pattern	—	—	(1.25)	(1.45)	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMIS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power consumption and power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 120 Hz, where as a power dissipation check pattern below is displayed.

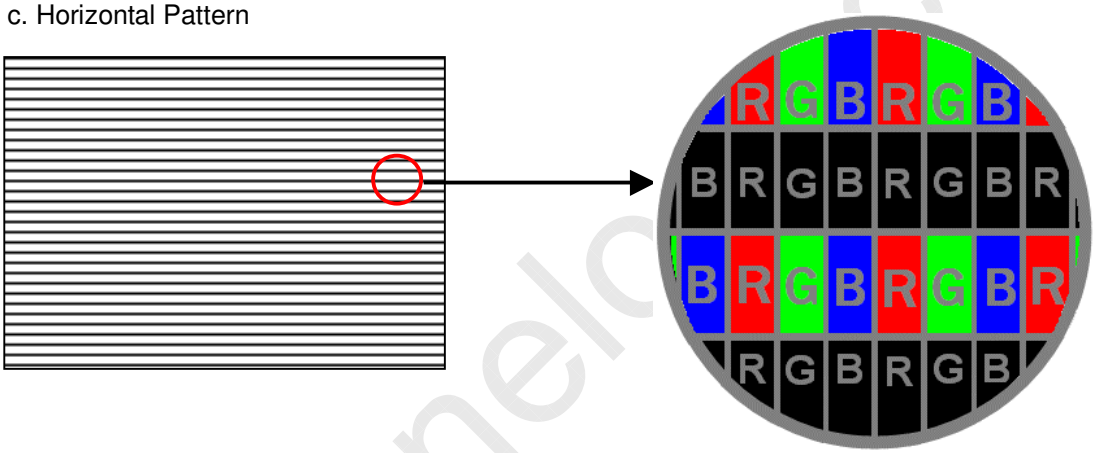
a. White Pattern

Active Area

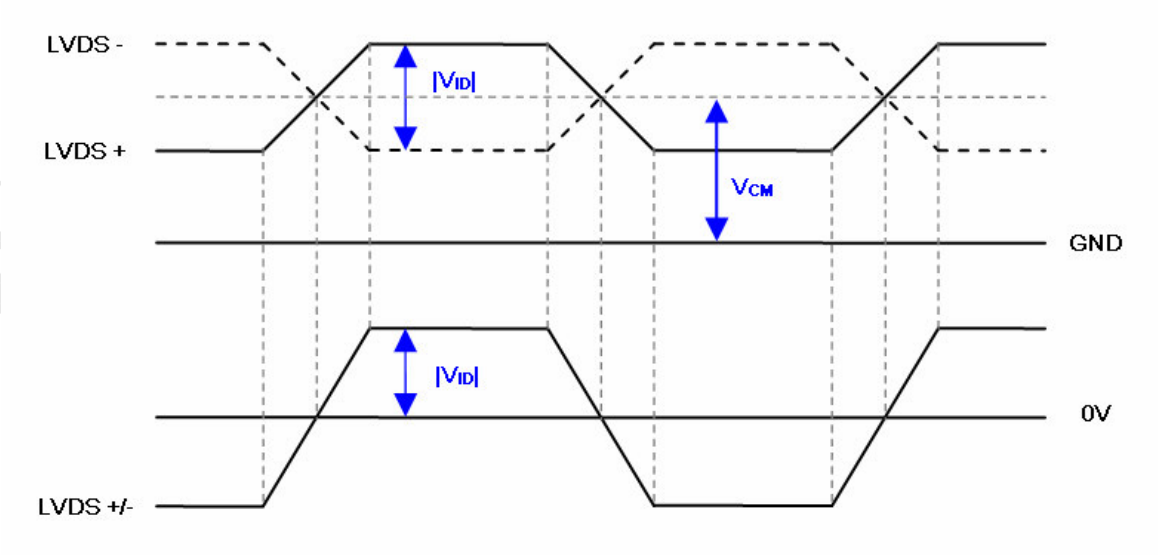
b. Black Pattern

Active Area

c. Horizontal Pattern

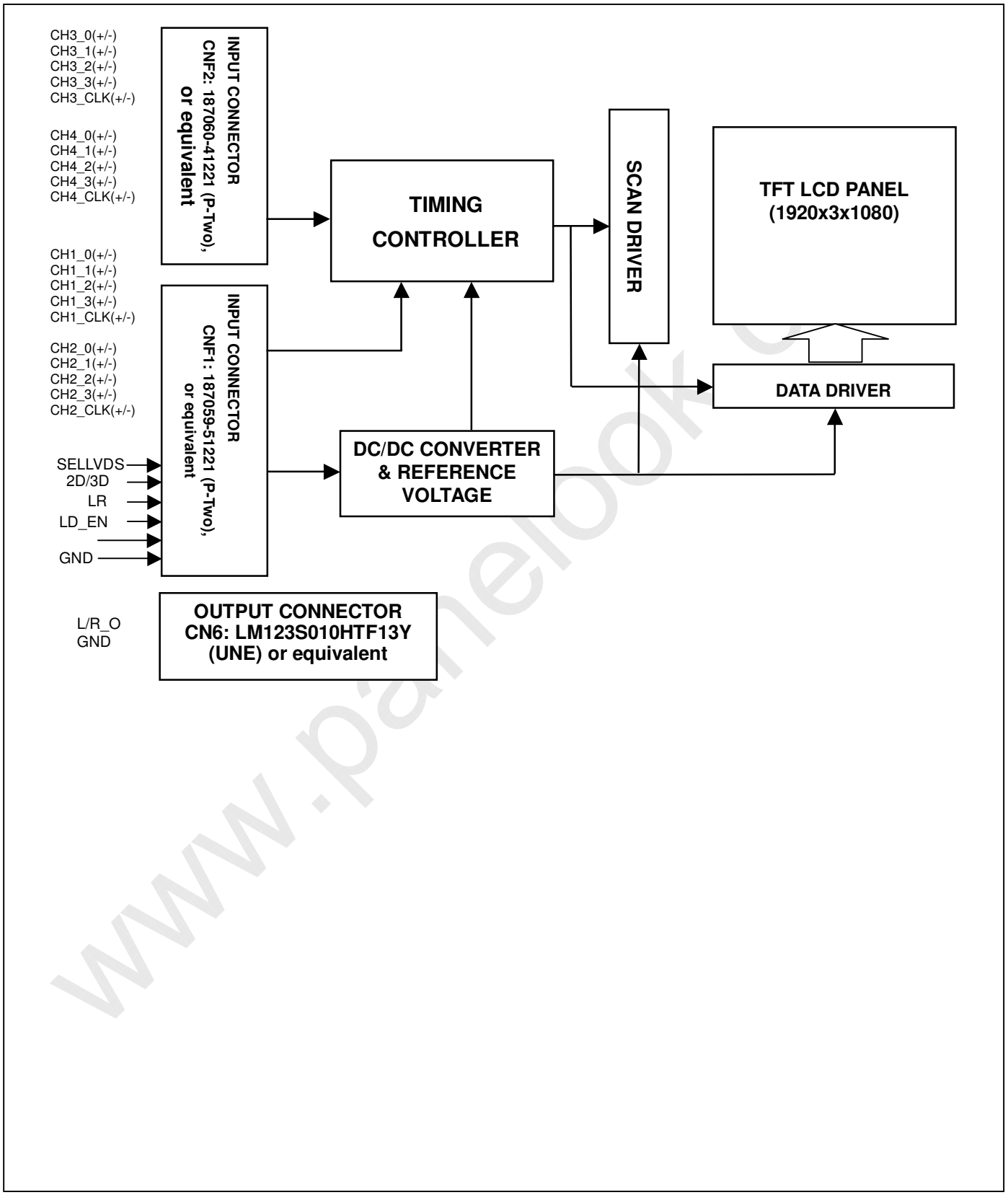


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Pin Assignment: (187059-51221 (P-Two) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	L/R_O	Output signal for Left Right Glasses control	(8)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)(6)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(6)
27	L/R	Input signal for Left Right eye frame synchronous	(4)(6)
28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	

29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	
42	LD_EN	Local Dimming Enable	(5)(6)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF2 Connector Pin Assignment (187060-41221 (P-Two) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	N.C.	No Connection	
23	N.C.	No Connection	
24	GND	Ground	
25	GND	Ground	
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	

31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32	GND	Ground	
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
38	N.C.	No Connection	
39	N.C.	No Connection	
40	GND	Ground	
41	GND	Ground	

CN6 Connector Pin Assignment (LM123S010HTF13Y (UNE) or equivalent)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(8)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V

SELLVDS	Note
L	JEDIA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Left Right synchronous signal for glasses.

V_{IL}=0~0.8, V_{IH}=2.0~3.3

LR	Note
L	Right synchronous signal
H	Left synchronous signal

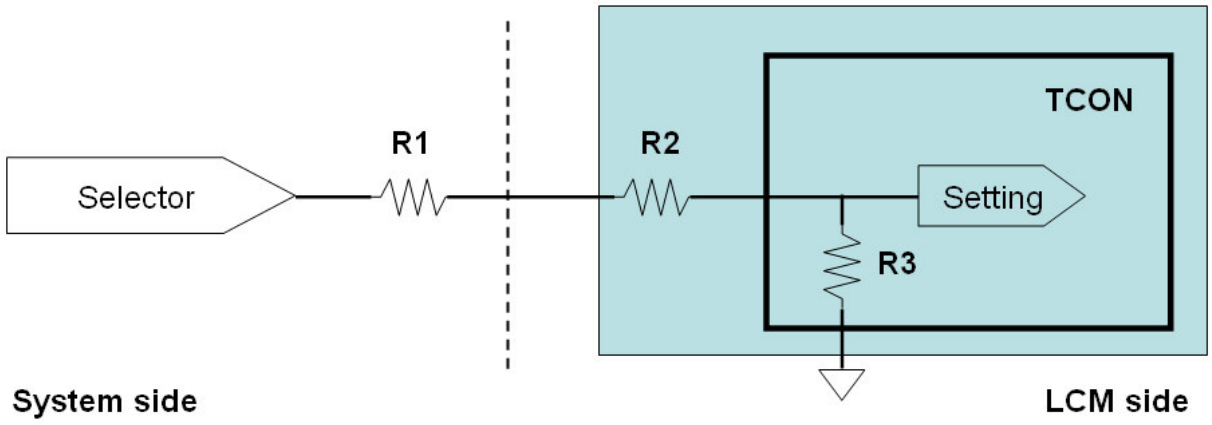
Note (5) Local dimming enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

LD_EN	Note
L or Open	Local Dimming Disable
H	Local Dimming Enable

Note (6) SELLVDS, 2D/3D, LR and LD_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



System side: R1 < 1K

Note (7) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

Note (8) The definition of L/R_O signal as follows

L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

Note (2) Reserved for internal use. Please leave it open.

Note (3) Low = Open or connect to GND: VESA Format, High = Connect to +3.3V: JEIDA Format.

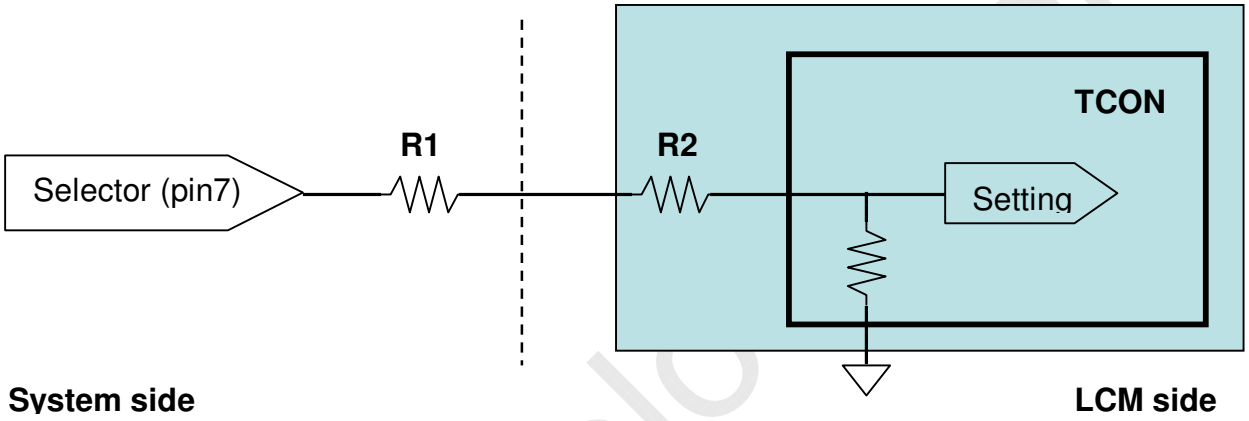
Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

Low = Open or connect to GND, High = Connect to +3.3V

ODSEL	Note
L or open	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (5) LVDS signal pin connected to the LCM side has the following diagram.

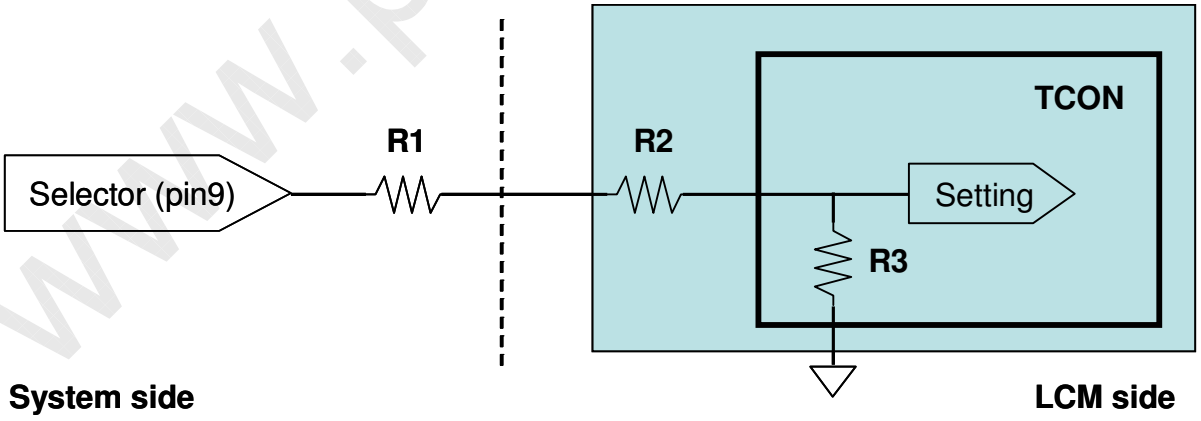
R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



System side: R1 < 1K

Note (6) ODSEL signal pin connected to the LCM side has the following diagram.

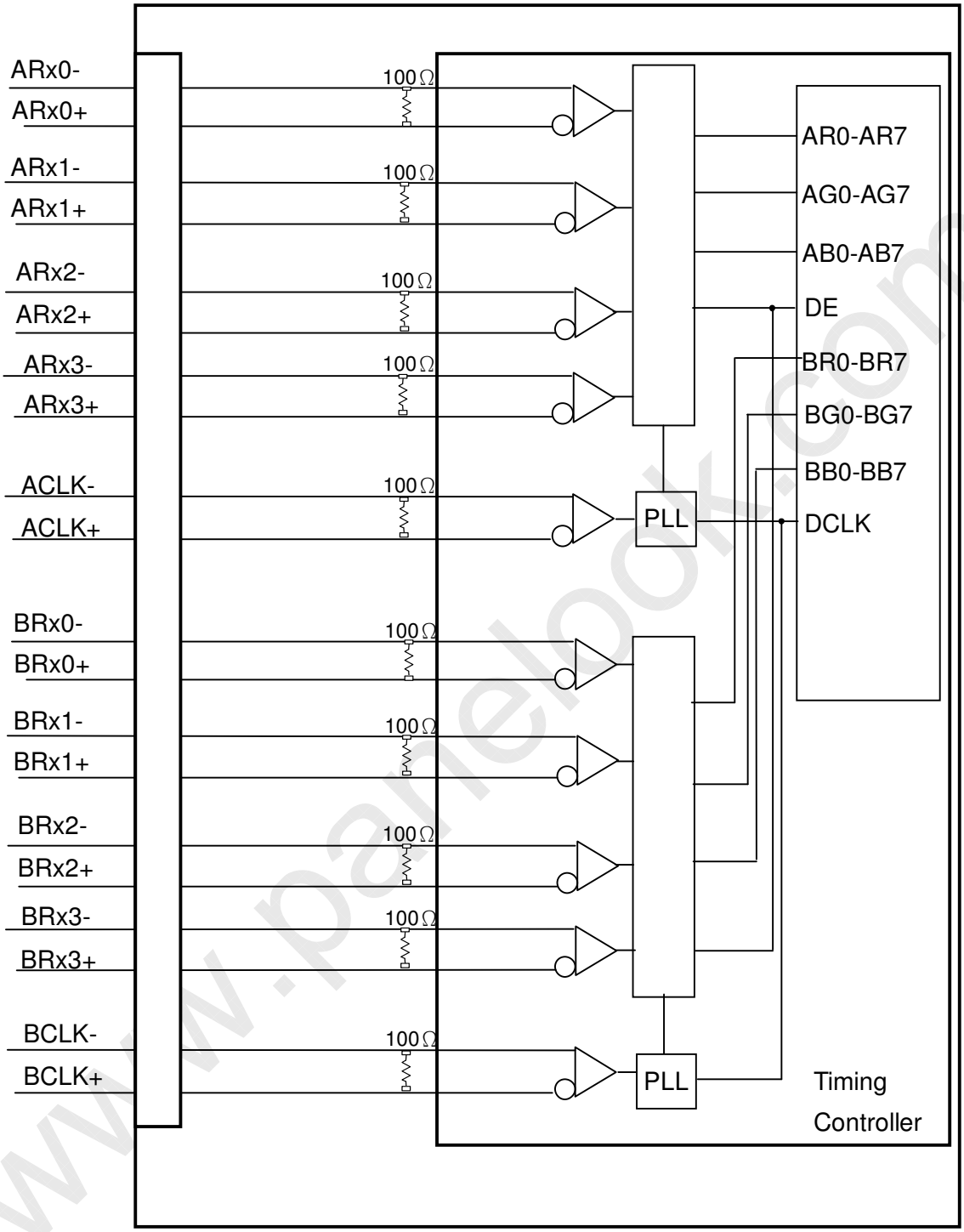
R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



Note (7) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

Note (8) The screw hole which is distant from the connector is merged with Ground

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR7	First pixel R data	BR0~BR7	Second pixel R data
AG0~AG7	First pixel G data	BG0~BG7	Second pixel G data
AB0~AB7	First pixel B data	BB0~BB7	Second pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR7	Third pixel R data	DR0~DR7	Fourth pixel R data
CG0~CG7	Third pixel G data	DG0~DG7	Fourth pixel G data
CB0~CB7	Third pixel B data	DB0~DB7	Fourth pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

Note (2) The system must have the transmitter to drive the module.

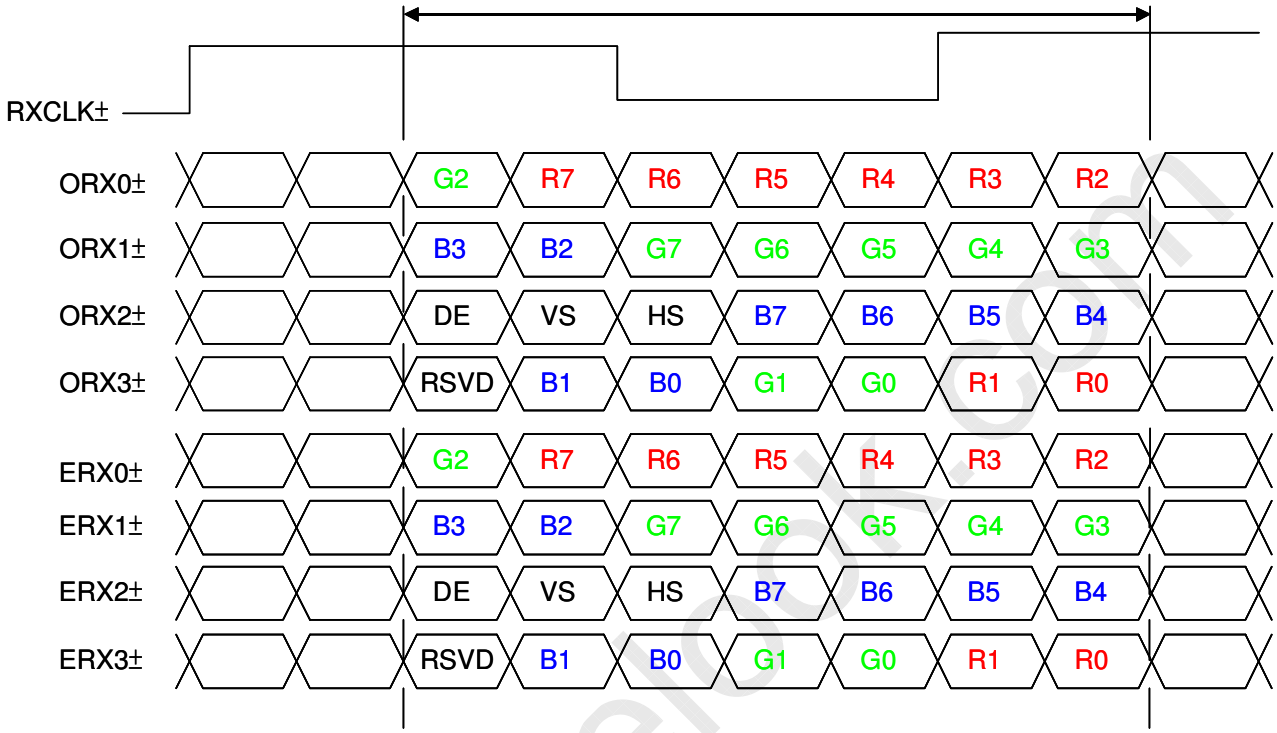
Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

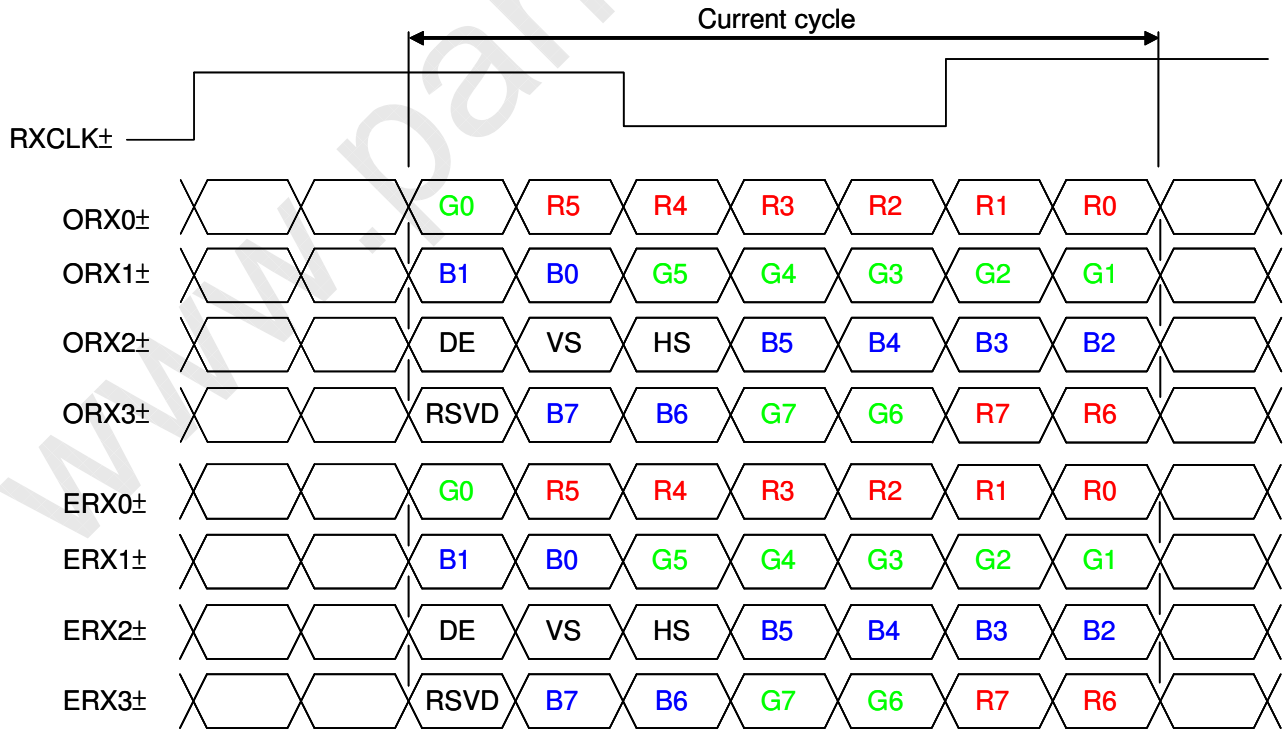
JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

JEDIA Format



VESA Format



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	96.012	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	(5)
	Hold Time	Tlvhd	600	-	-	ps	

6.1.1 Timing spec for Frame Rate (F_{r5} = 100Hz)

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	94	100	106	Hz	
	3D mode		F_{r5}	100	100	100	Hz	
Vertical Active Display Term	2D Mode	Total	Tv	1090	1125	1480	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	45	400	Th	—
	3D Mdoe	Total	Tv	1524			Th	(6)
		Display	Tvd	1080			Th	
		Blank	Tvb	444			Th	
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—
	3D Mdoe	Total	Th	525			Tc	(6)
		Display	Thd	480			Tc	
		Blank	Thb	45			Tc	

6.1.2 Timing spec for Frame Rate (F_{r6} = 120Hz)

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	114	120	126	Hz	
	3D mode		F_{r6}	120	120	120	Hz	
Vertical Active Display Term	2D Mode	Total	Tv	1090	1125	1480	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	45	400	Th	—
	3D Mdoe	Total	Tv	1524				(6)
		Display	Tvd	1080				
		Blank	Tvb	444				
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—
	3D Mdoe	Total	Th	525				(6)
		Display	Thd	480				
		Blank	Thb	45				

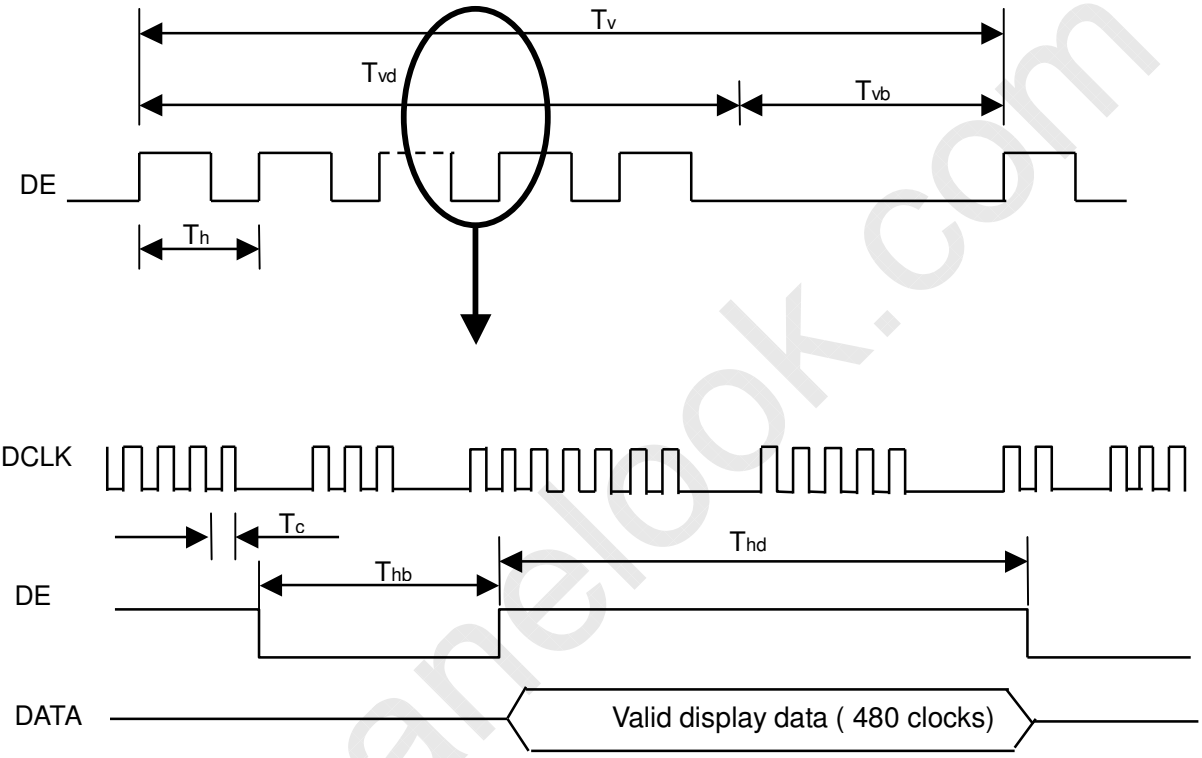
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

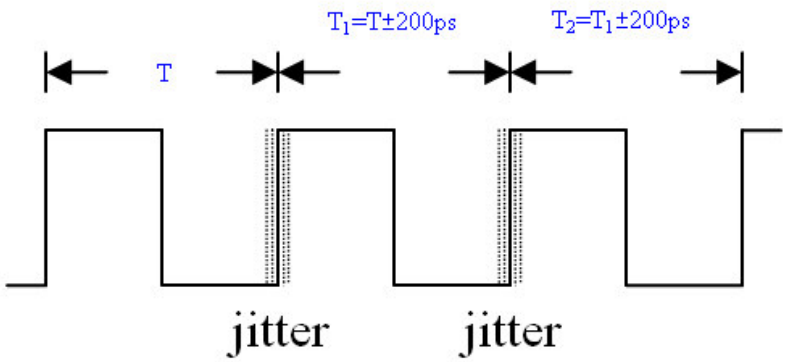
$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

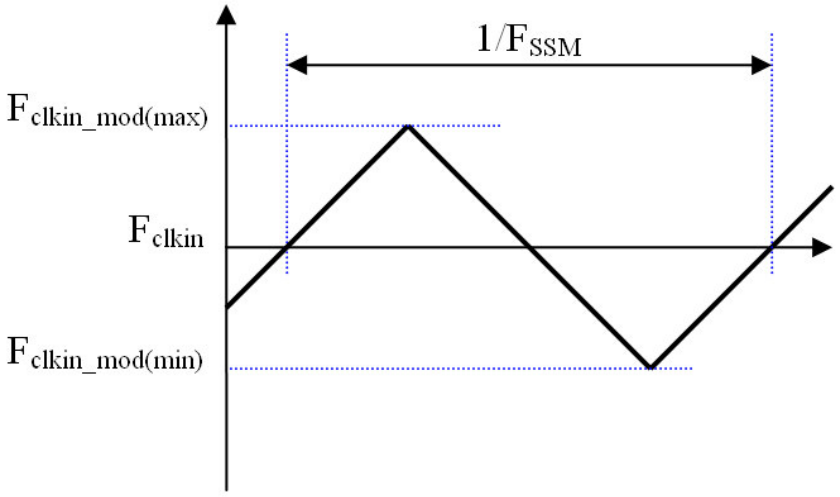
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

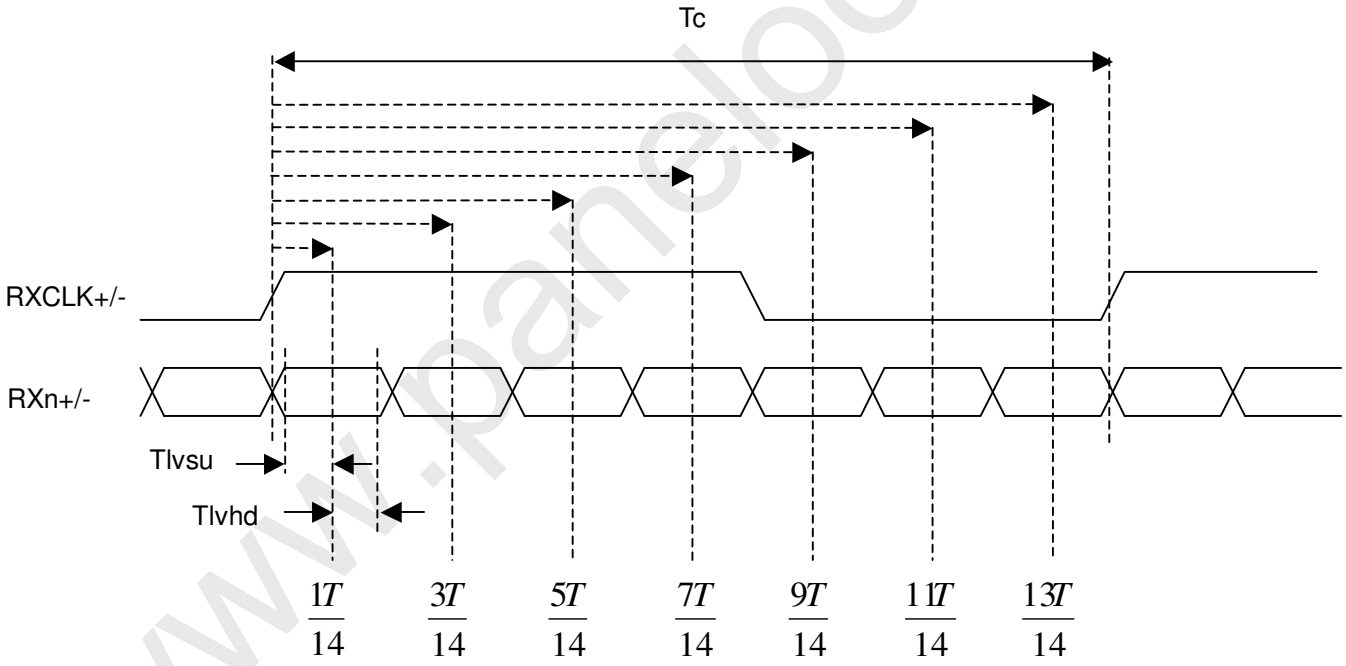


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) Please fix the Vertical timing (Vertical Total =1524 / Display =1080 / Blank = 444) in 3D mode.

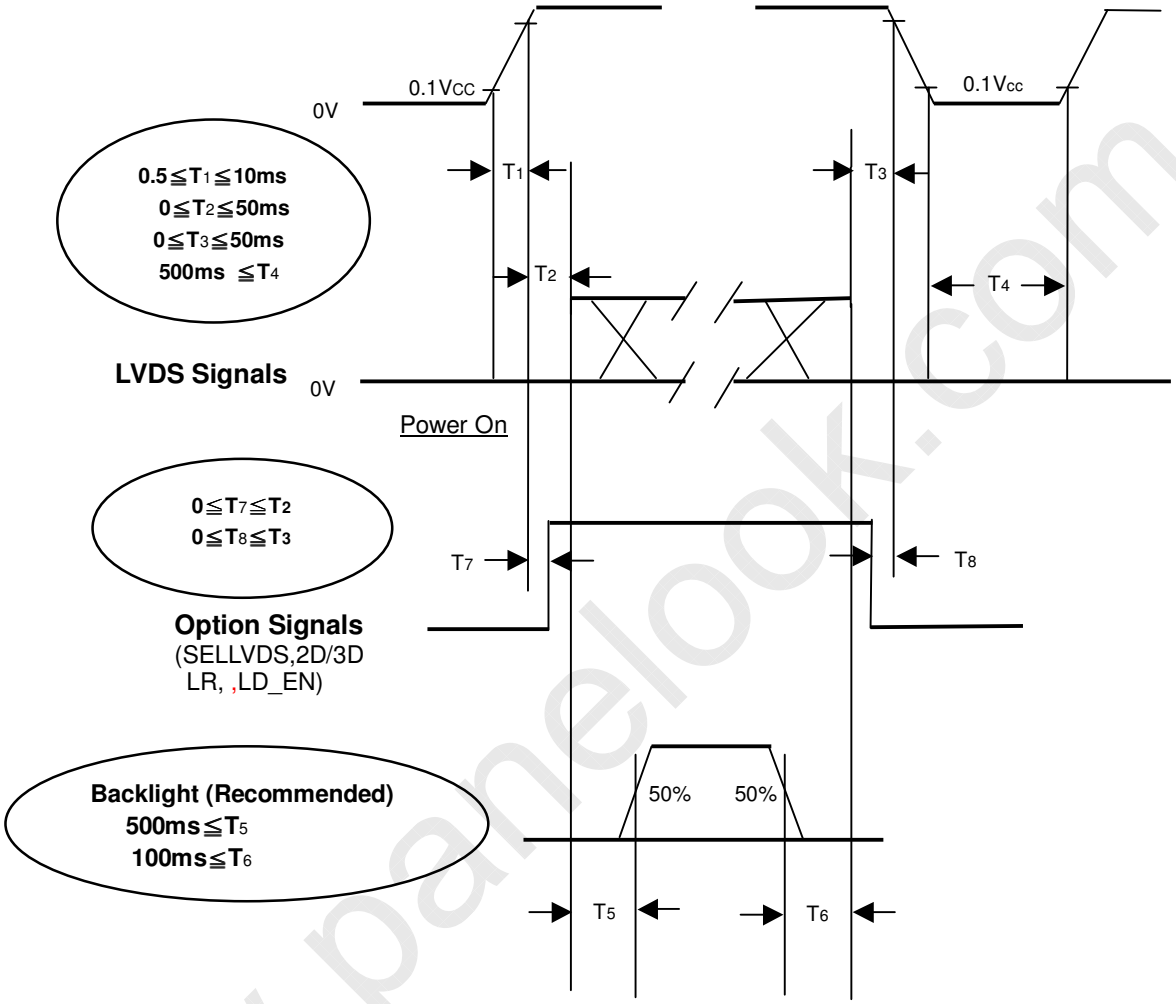
Please fix the Horizontal timing (Horizontal Total =525 / Display =480 / Blank = 45) in 3D mode.

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

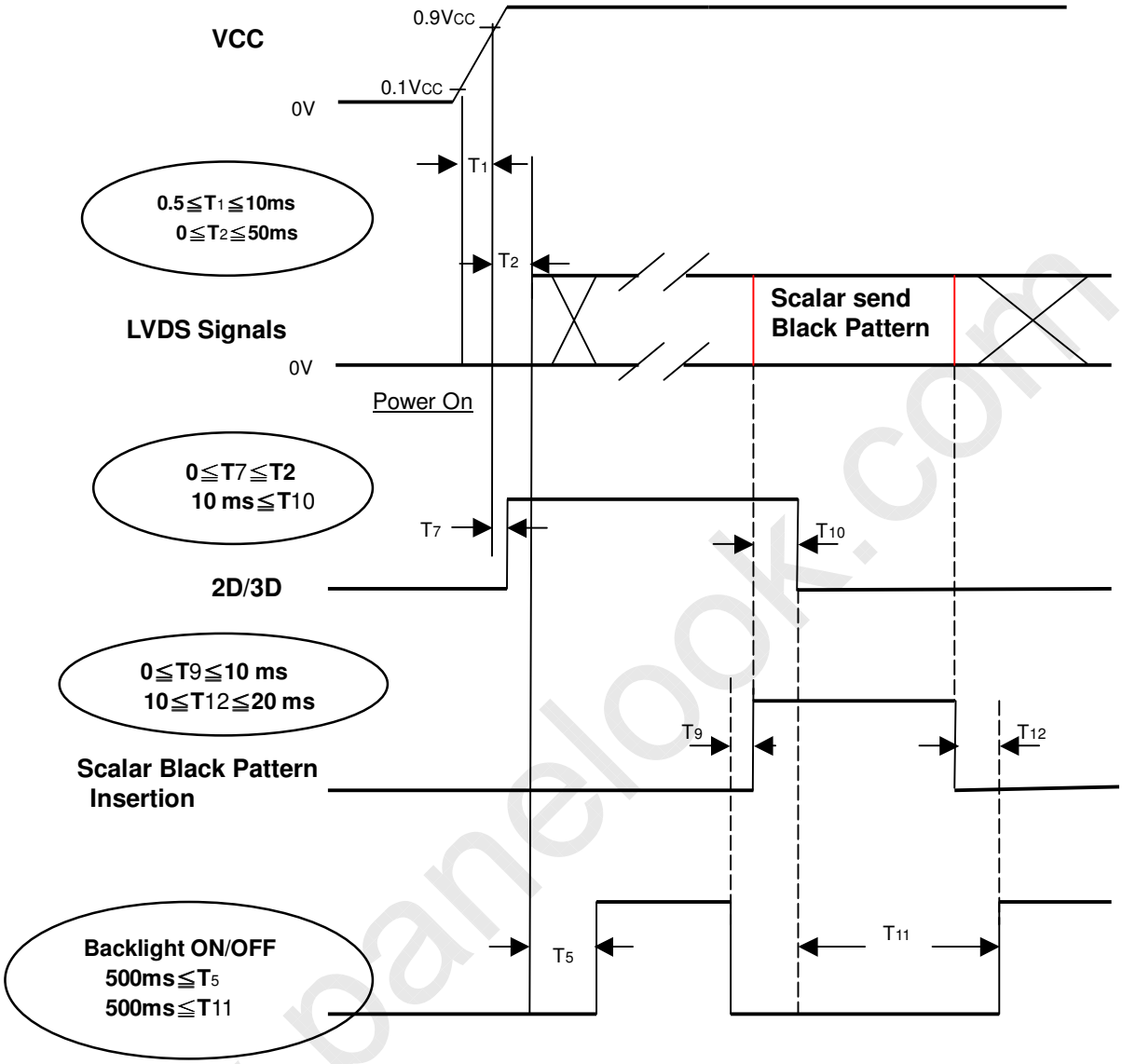
6.2.1 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

6.2.2 2D to 3D SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

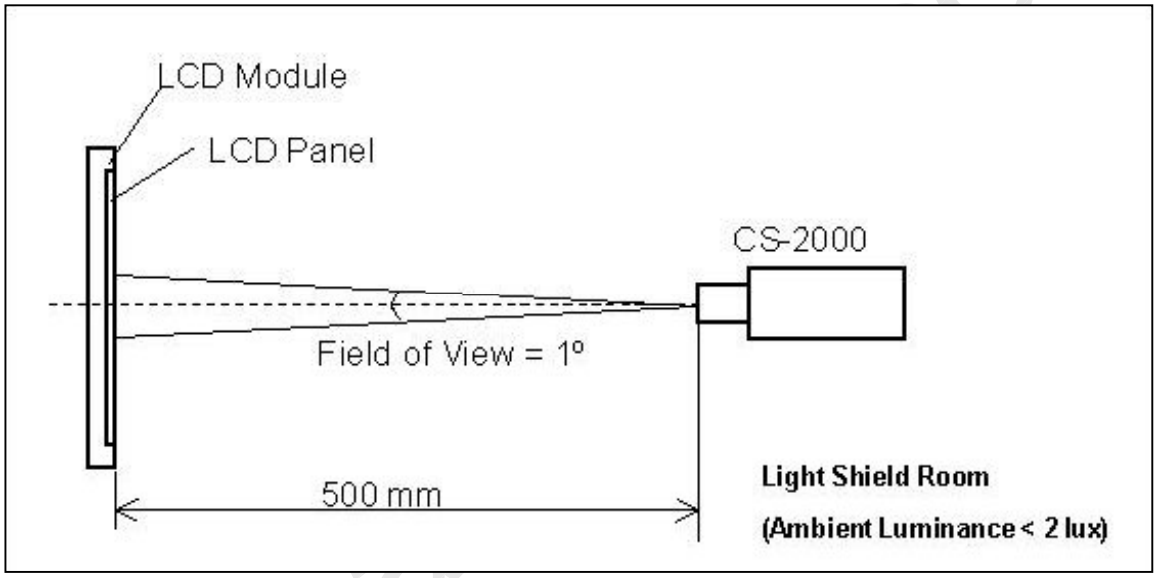
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I_L	130±7.8	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



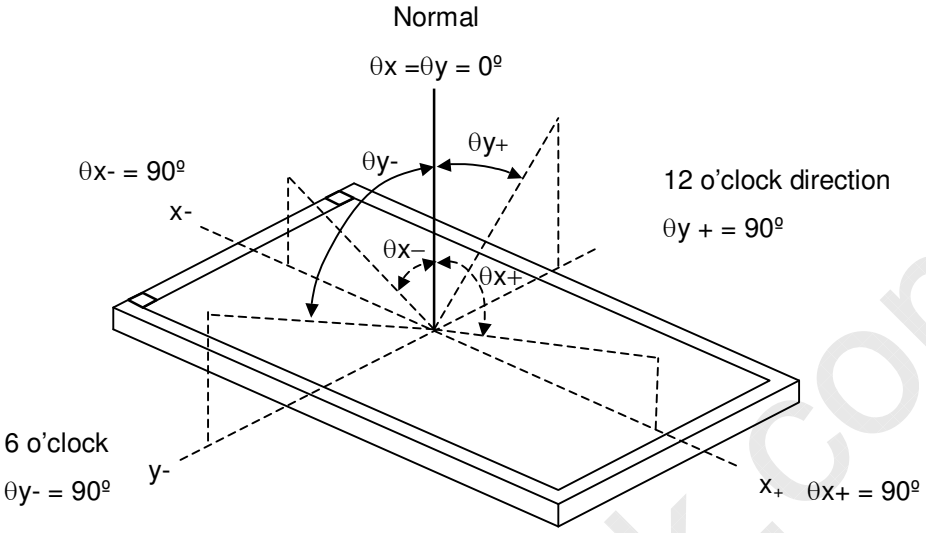
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction		(1000)	-	-	(2)
Response Time (TN)		T_R		-	(1.1)	-	ms	(3)
		T_F		-	(3.2)	-	ms	
Center Luminance of White		2D L_C		(350)	(400)	-	cd/m^2	(4)
		3D L_C		-	(45)	-		
White Variation		δW		-	-	1.3	-	(6)
Cross Talk		2D		-	-	4	%	(5)
		3D_W			(4)			(8)
		3D_D			(11)			(8)
Color Chromaticity	Red	Rx		Typ. -0.03	(0.647)	Typ. +0.03	-	-
		Ry			(0.328)		-	
	Green	Gx			(0.279)		-	
		Gy			(0.633)		-	
	Blue	Bx			(0.154)		-	
		By			(0.058)		-	
	White	Wx			(0.280)		-	
		Wy			(0.290)		-	
	Color Gamut	C.G		-	(72)	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥10 (TN)		(80)	-	Deg.	(1)
		θx-			(80)	-		
	Vertical	θY+			(80)	-		
		θY-			(70)	-		
Transmission direction of up polarizer		ϕ_{up}			90		Deg	(7)

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

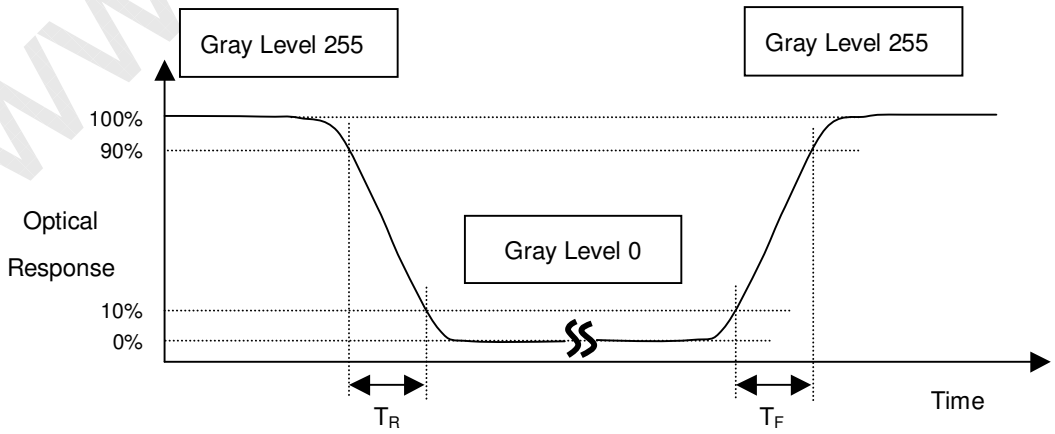
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

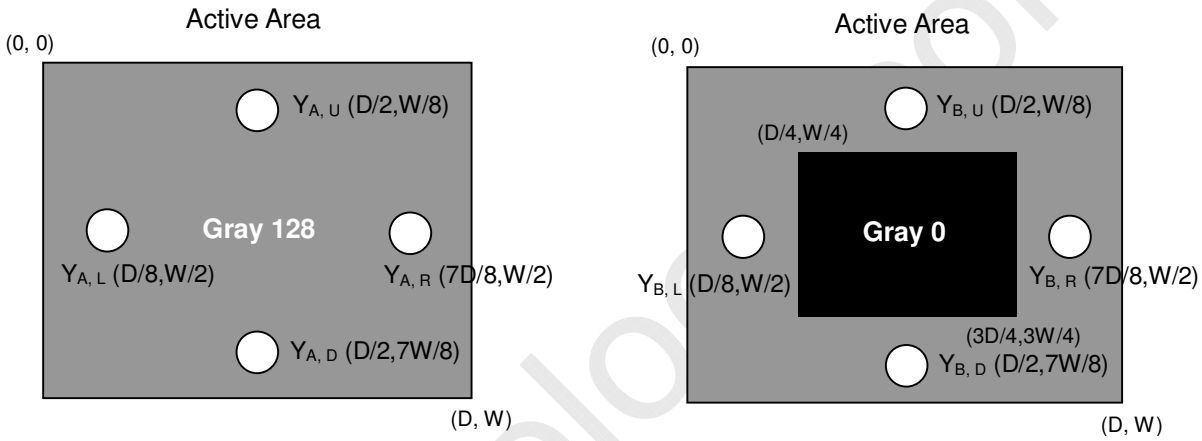
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

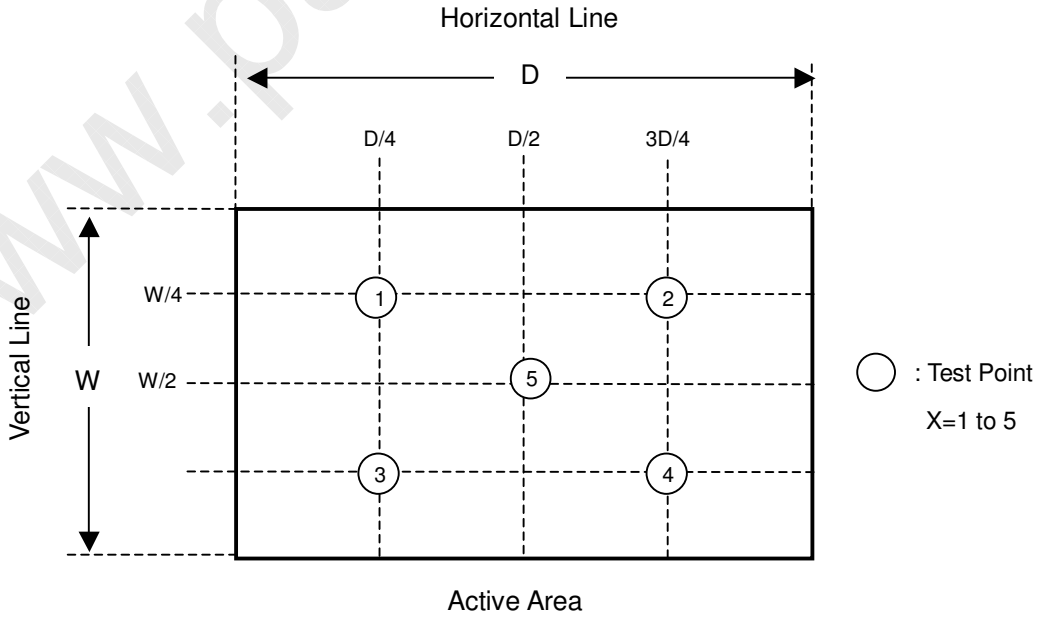
Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

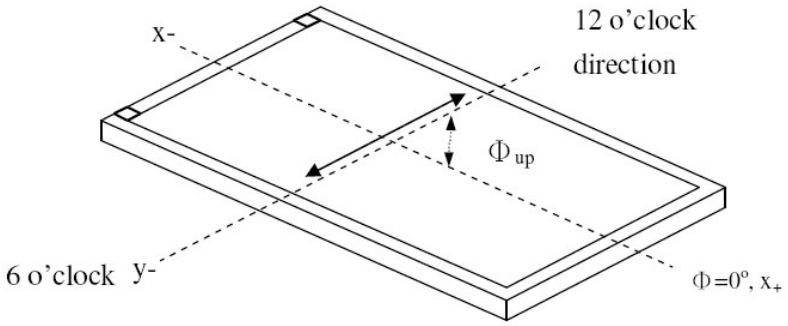
Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]

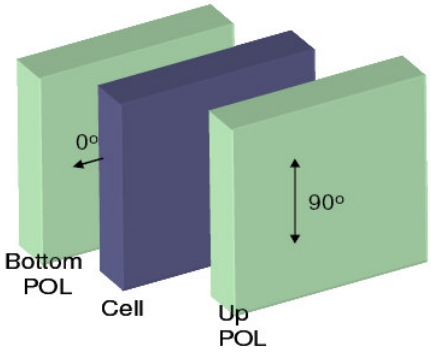


Note (7) This is a reference for designing the shutter glasses of 3D application.

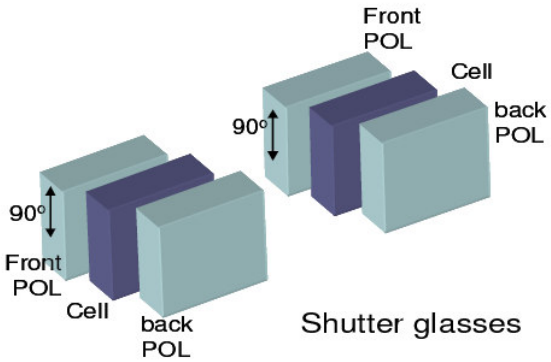
Definition of the transmission direction of the up polarizer:



The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



LCD module

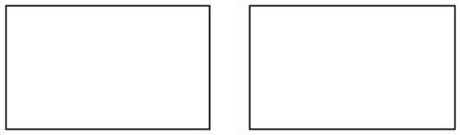


Shutter glasses

Note (8) Definition of the 3D mode performance (measured under 3D mode):

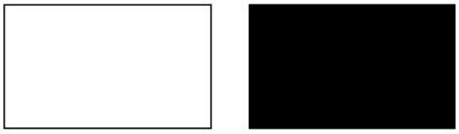
a. Test pattern

Left eye image and right eye image are displayed alternated



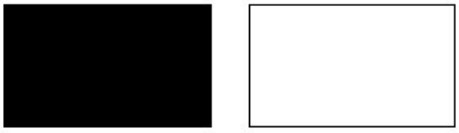
WW

Left eye image: W255; Right eye image: W255



WB

Left eye image: W255; Right eye image: W0



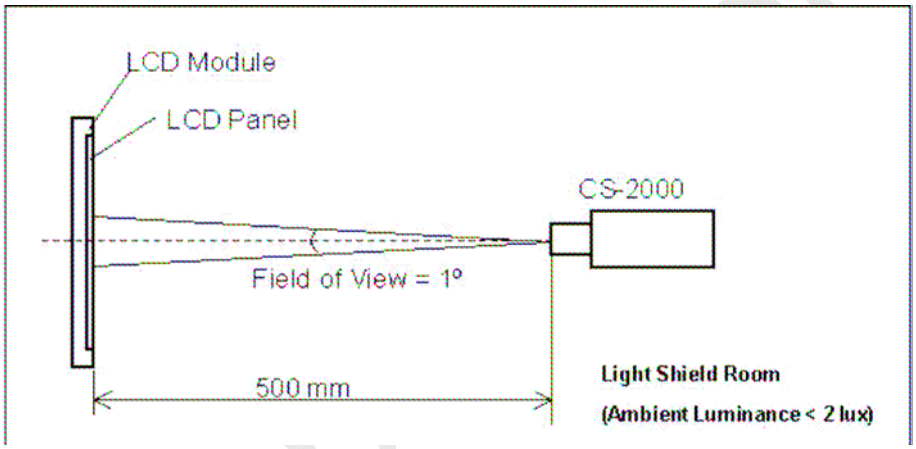
BW

Left eye image: W0; Right eye image: W255

BB

Left eye image: W0; Right eye image: W0

b. Measurement Setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. "The transmittance of the glass should be larger than 40.0% under 3D mode operation."

The luminance of the test pattern “WW”, denoted L(WW); the luminance of the test pattern ”WB”, denoted L(WB); the luminance of the test pattern “BW”, denoted L(BW); the luminance of the test pattern “BB”, denoted “L(BB)

c. Definition of the Center Luminance of White, Lc (3D) : L(WW)

d. Definition of the 3D mode white crosstalk, CT (3D-W)

$$CT(3D-W) \equiv \left| \frac{L(WB) - L(BB)}{L(WW) - L(BB)} \right|$$

e. Definition of the 3D mode dark crosstalk, CT (3D-D)

$$CT(3D-D) \equiv \left| \frac{L(WW) - L(BW)}{L(WW) - L(BB)} \right|$$

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMIS LSI chips.

[5] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.

[6] Do not plug in or pull out the I/F connector while the module is in operation.

[7] Do not disassemble the module.

[8] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[9] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[10] When storing modules as spares for a long time, the following precaution is necessary.

[10.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[10.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[11] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

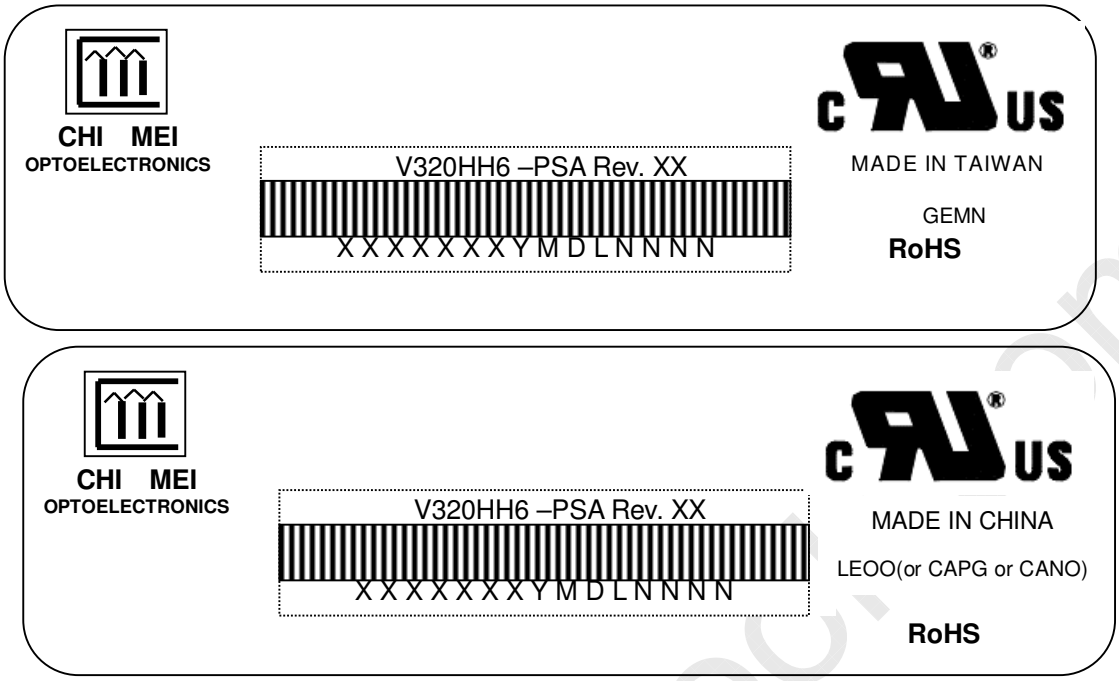
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMO MODULE LABEL

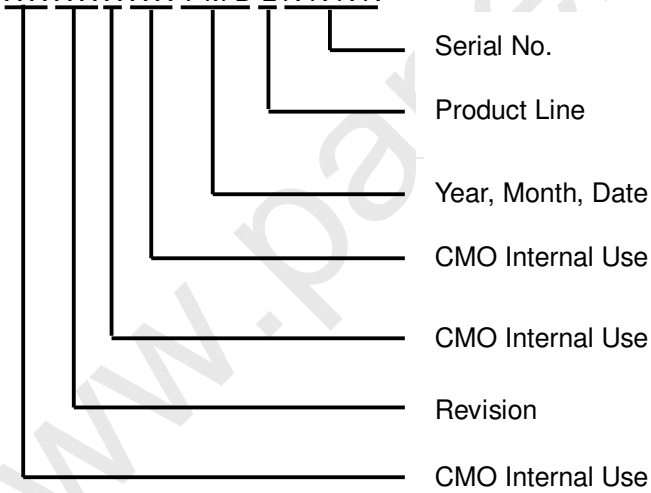
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V320HH6-PSA

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

Product Line: 1 -> Line1, 2 -> Line 2, …etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 18 LCD TV Panels / 1 Box

(2) Box dimensions : 970 (L) X 640 (W) X 319 (H)

(3) Weight : approximately 36Kg (18 panels per box)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

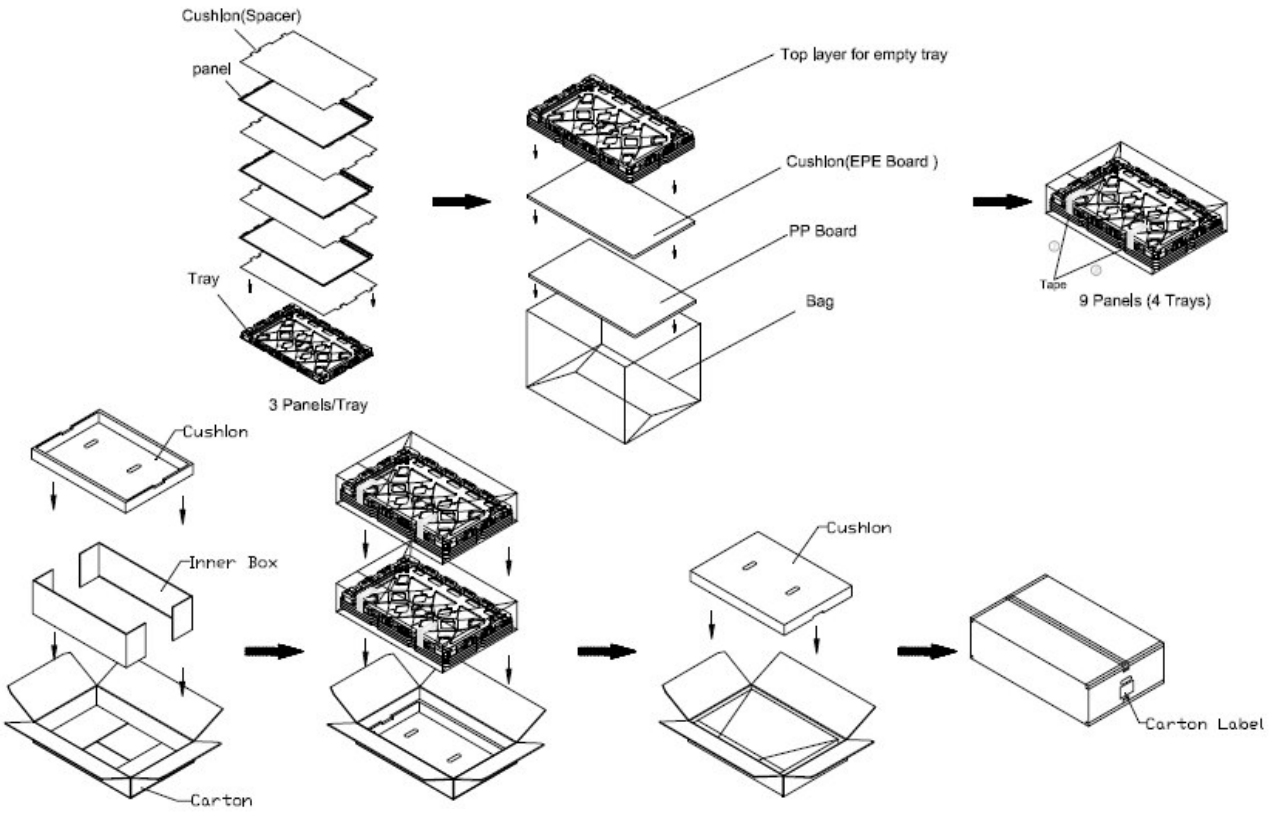
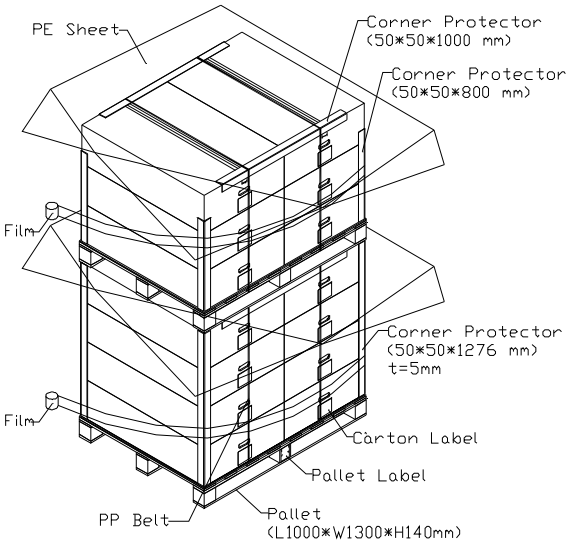
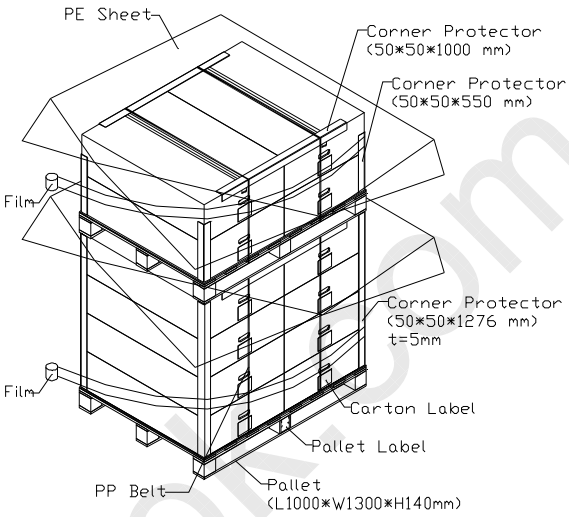


Figure.10-1 packing method

Sea / Land Transportation
(40ft HQ Container)



Sea / Land Transportation
(40ft Container)



Air Transportation

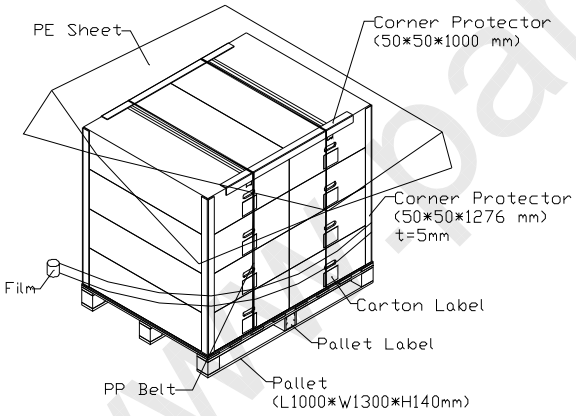


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTIC